Plan for CD-1 review and further
including FEE update

Takao Sakaguchi

Topics to be discussed

- Overview of overall schedule
  - Schedule of prototype development
  - Schedule of mass production
- Status and issue of FEE
  - DAM/EBDC part will be presented by Jin
- How to test FEE and DAM/EBDC
  - Test stand development idea
  - Mass test scheme for production
- Costs review for CD-1 review
  - Prototype costs
  - Mass production costs

Schedules and funding news

- All the development should be finished by Jul 2018
  - Pre-prototype, prototype v1 and pre-production prototype

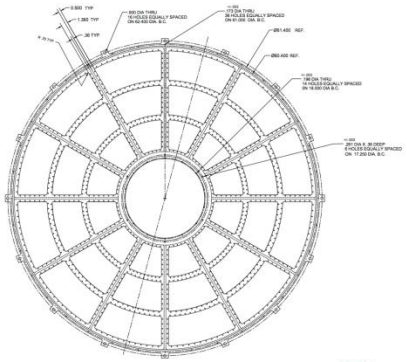
- Use of OPC fund is just approved
  - Enough funding for all the prototype development
  - $90K for FEE, $40K for DAM/EBDC

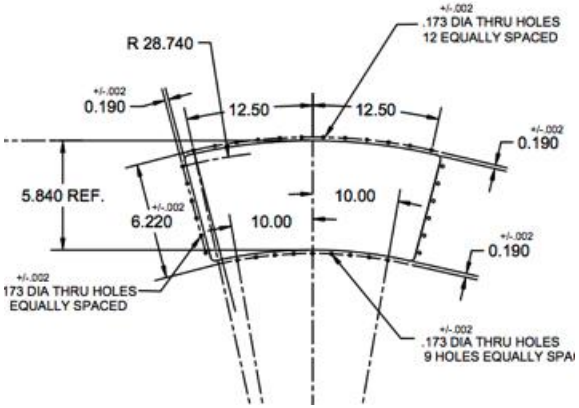
sPHENIX PROJECT SCHEDULE (Modified to fit updated DOE/CD Milestones)

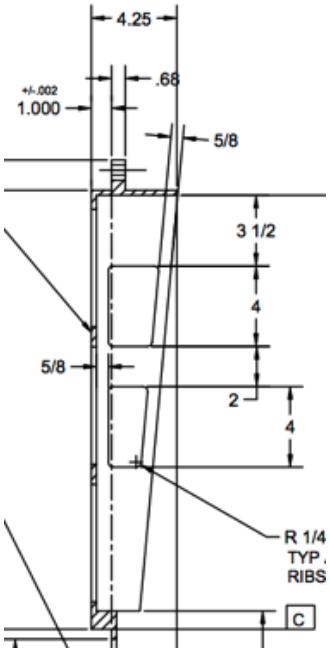
WBS	Task Name	Duration	Start	Finish	Predecessors	Successors	Resource Names	Fixed Cost
1.2.6	**TPC FEE**	**696 days**	**Thu 9/22/16**	**Wed 7/10/19**				**$0**
1.2.6.1	**TPC FEE Prototype v1**	**230 days**	**Thu 9/22/16**	**Wed 8/23/17**				**$0**
1.2.6.1.1	Write TPC FEE prototype v1 design specification	10 days	Thu 9/22/16	Wed 10/5/16	2	183	SCI3 PO[30%],PROF4 PO E[35%],TECH3 PO D[35%]	$0
1.2.6.1.2	Design TPC FEE protoype v1	135 days	Thu 10/6/16	Fri 4/21/17	182	184,186,187	PROF4 PO E[50%],TECH3 PO D[50%]	$0
1.2.6.1.3	Procure TPC FEE prototype v1 components	15 days	Mon 4/24/17	Fri 5/12/17	183	185	PROF4 PO E[10%]	$11,000
1.2.6.1.4	Fabricate TPC FEE prototype v1 boards	30 days	Mon 5/15/17	Mon 6/26/17	184	188	PROF4 PO E[10%]	$8,000
1.2.6.1.5	Procure TPC FEE prototype v1 LV power supplies	5 days	Mon 4/24/17	Fri 4/28/17	183	188	SCI3 PO[10%],PROF4 PO E[10%],TECH3 PO D[10%]	$12,000
1.2.6.1.6	Develop TPC FEE Test Stand	40 days	Mon 4/24/17	Mon 6/19/17	183	188	SCI3 PO[10%],PROF4 PO E[25%],TECH3 PO D[30%],TECH3 PO E[	$150,000
1.2.6.1.7	Assemble and test TPC FEE prototype v1	40 days	Tue 6/27/17	Wed 8/23/17	187,186,185	190	SCI3 PO[10%],PROF4 PO E[20%],TECH3 PO D[20%],TECH3 PO E[	$2,000
1.2.6.2	**TPC FEE Pre-Production**	**155 days**	**Thu 8/24/17**	**Tue 4/10/18**				**$0**
1.2.6.2.1	Design TPC FEE preproduction protoype	70 days	Thu 8/24/17	Tue 12/5/17	188	191,193	PROF4 PO E[50%],TECH3 PO D[50%]	$0
1.2.6.2.2	Procure TPC FEE preproducion prototype compor	15 days	Wed 12/6/17	Thu 12/28/17	190,4	192	PROF4 PO E[10%]	$11,000
1.2.6.2.3	Fabricate TPC FEE preproduction prototype boar	30 days	Fri 12/29/17	Mon 2/12/18	191	194	PROF4 PO E[10%]	$8,000
1.2.6.2.4	Modify TPC FEE Test Stand	30 days	Wed 12/6/17	Mon 1/22/18	190	194	SCI3 PO[10%],PROF4 PO M[25%],TECH3 PO D[30%],TECH3 PO E[	$8,000
1.2.6.2.5	Assemble and test TPC FEE preproduction protot	40 days	Tue 2/13/18	Tue 4/10/18	193,192	196	SCI3 PO[10%],PROF4 PO E[20%],TECH3 PO D[20%],TECH3 PO E[	$2,000
1.2.6.3	**TPC FEE Production**	**212 days**	**Fri 8/31/18**	**Wed 7/10/19**				**$0**
1.2.6.3.1	Procure TPC FEE components	70 days	Fri 8/31/18	Thu 1/31/19	6,194	198	SCI3 Other[10%],PROF4 PO E[50%],TECH3 PO D[40%]	$221,000
1.2.6.3.2	Procure TPC FEE LV power supplies	40 days	Fri 8/31/18	Fri 10/26/18	6		PROF4 PO E[10%]	$84,000
1.2.6.3.3	Fabricate and assemble all TPC Fee boards	55 days	Fri 2/1/19	Fri 4/19/19	196	200	PROF4 PO E[10%]	$200,000
1.2.6.3.4	Procure TPC FEE Optical Fibers	40 days	Fri 8/31/18	Fri 10/26/18	6	200	PROF4 PO E[10%]	$100,000
1.2.6.3.5	Perform QA Testing on TPC FEE	55 days	Mon 4/22/19	Wed 7/10/19	198,199	118	SCI3 Other[10%],PROF4 PO E[10%],TECH3 Other[30%],STUDENT	$0
1.2.7	**TPC DAM**	**734 days**	**Thu 9/22/16**	**Tue 9/3/19**				**$0**
1.2.7.1	**TPC DAM Evaluation --FELIX 1.5**	**180 days**	**Thu 9/22/16**	**Mon 6/12/17**				**$0**
1.2.7.1.1	Write Design Spec for TPC DAM prototype v1	110 days	Thu 9/22/16	Fri 3/3/17	2	204	SCI3 PO[30%],PROF4 PO E[35%],TECH3 PO D[35%]	$0
1.2.7.1.2	Develop TPC DAM prototype v1 Test Stand	40 days	Mon 3/6/17	Fri 4/28/17	203	205	PROF4 PO E[50%],TECH3 PO D[50%]	$12,000
1.2.7.1.3	Measure TPC DAM prototype v1 Throughput	30 days	Mon 5/1/17	Mon 6/12/17	204		PROF4 PO E[50%],TECH3 PO D[50%]	$0
1.2.7.2	**TPC DAM Evaluation -- FELIX 2.0**	**105 days**	**Mon 12/4/17**	**Fri 5/4/18**				**$0**
1.2.7.2.1	Procure FELIX 2.0 board for TPC DAM	15 days	Mon 12/4/17	Tue 12/26/17	4	208	PROF4 PO E[10%]	$12,000
1.2.7.2.2	Measure Throughput of FELIX 2.0 for TPC DAM	30 days	Wed 12/27/17	Thu 2/8/18	207	209	PROF4 PO E[10%]	$0
1.2.7.2.3	Develop TPC DAM FPGA Algorithm	60 days	Fri 2/9/18	Fri 5/4/18	208		SCI3 Other[10%],PROF4 PO E[25%],TECH3 PO D[30%],TECH3 PC	$0
1.2.7.3	**TPC DAM Production**	**250 days**	**Fri 8/31/18**	**Tue 9/3/19**				**$0**
1.2.7.3.1	Procure TPC DAM Felix 2.0 boards	75 days	Fri 8/31/18	Wed 12/19/18	6	212	SCI3 Other[10%],PROF4 PO E[50%],TECH3 PO D[40%]	$300,000
1.2.7.3.2	Perform QA Testing on TPC DAM FELIX 2.0 boards	55 days	Thu 12/20/18	Wed 3/13/19	211	214	SCI3 Other[10%],PROF4 PO E[10%],TECH3 PO E[30%],STUDENT[	$0
1.2.7.3.3	Procure of TPC EDBC Computers and Peripherals	60 days	Fri 8/31/18	Mon 11/26/18	6	214	SCI3 Other[30%],PROF4 PO E[40%],TECH3 PO D[30%]	$150,000
1.2.7.3.4	Test Full TPC DAM System	120 days	Thu 3/14/19	Tue 9/3/19	213,212		SCI3 Other[50%],PROF4 PO E[50%]	$0

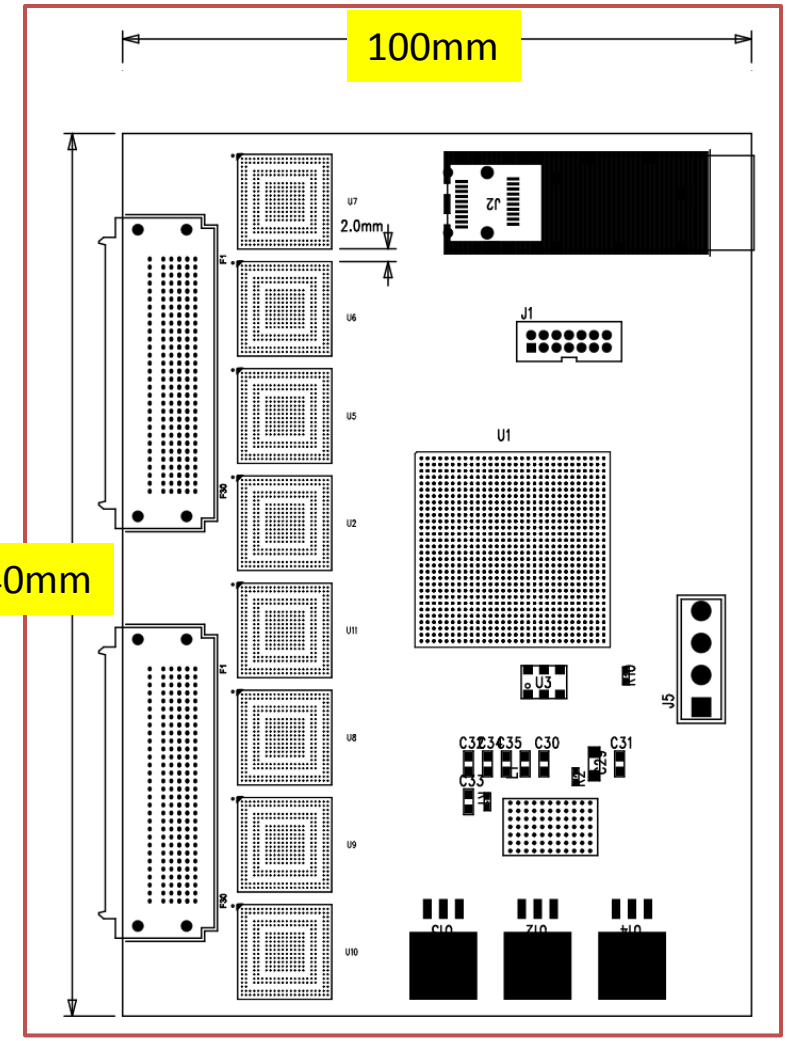
Status of FEE (I)

- Joe produced initial board layout with eight SAMPAs
- It fits to the support structure at the endcap
  - Board width should be <14.8cm
  - Board length should be <10cm
  - Board spacing should be <2cm









Status of FEE (II)

- Decided produceing a pre-prototype board for FEE
  - Just 2 SAMPAs with a Xilinx Attira-7 chip (basic testing purpose)
  - Time scale: ~3d (design) + 4w (layout) + 2w (fab) + 1w (parts mount)
  - Work on real prototype in parallel to the pre-prototype production

- Expect ~2-4 SAMPA chips (MPW2) from STAR (Tonko)
  - Tonko will inform us later how many chips exactly he can provide us
  - These chips are for pre-prototype board
  - Also asking Chuck Britton of ORNL and David Silvermyr for more

- ~200 SAMPA chips (still MPW2) are expected in May
  - Tonko will purchase 400 chips for iTPC. However, he said that he won't use more than 200. Another 200 will be for us

- There is not issue for SAMPA chip acquisition for mass production
  - Maro Bregant of Universidade de Sao Paulo assured this

Radiation

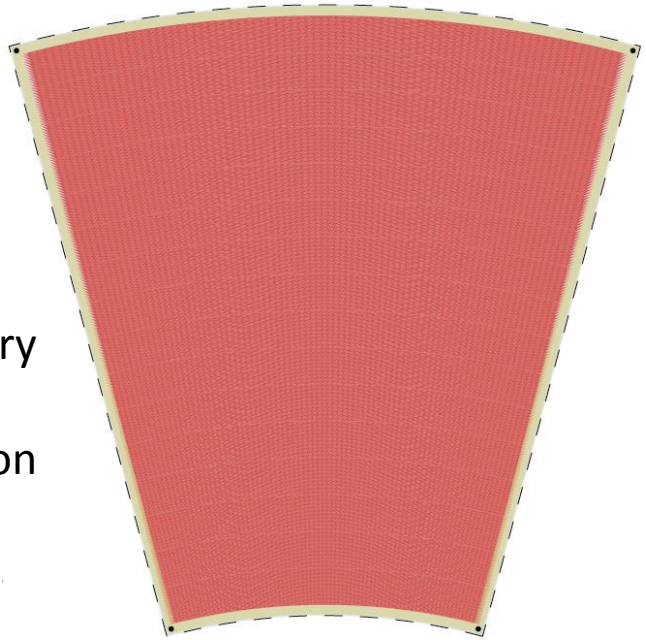
- Initial radiation estimate is estimated
  - Eric's analysis result of RadFET monitoring during Run-14 Au+Au 200GeV run
  - Delivered luminosity to PHENIX was 23 nb^{-1}
- Measured result
  - 100Gy at r=3.5cm, 50Gy at r=6.5cm, 15Gy at r=16cm
  - Simple $1/r^2$ dependence
- Total Dose at TPC (@100KHz): 10μGy/sec at 16cm
  - Highest radiation possible at TPC
- Neutron flux is being estimated by Eric

Current pad design

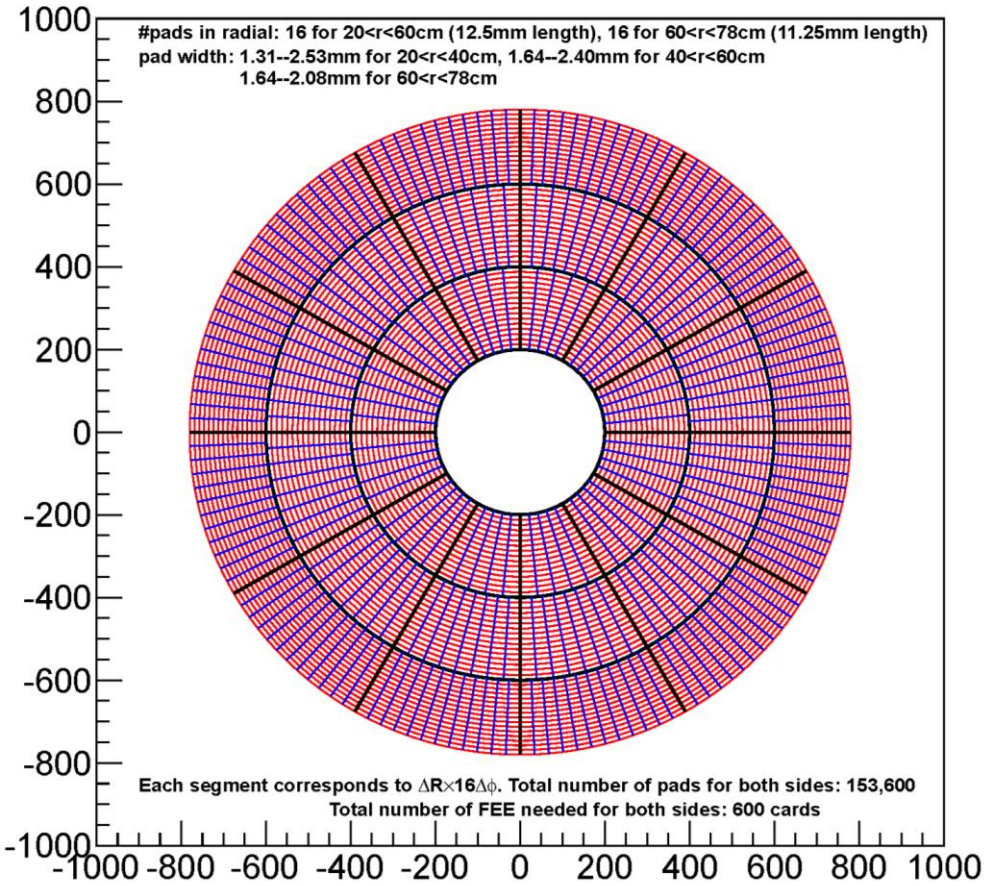
- Three segments in radial direction, each divided into 16
  - 12 sectors in phi direction, each divided into multiple of 16
- Each cell in the right figure corresponds to 16 pads in phi
  - Zigzag-type pad configuration

5 FEEs for 20<r<40cm, 8 for 40<r<60cm, 12 for 60<r<78cm, for each 1/12 of full azimuth

Each cell = 16pads in phi

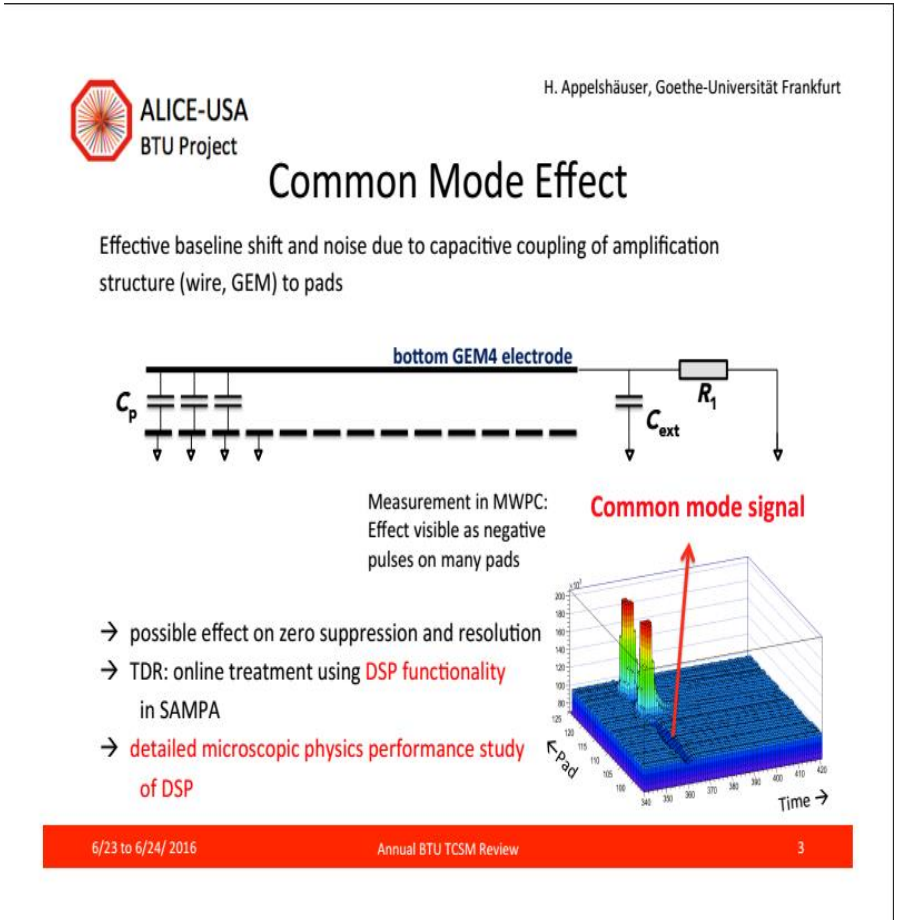


Preliminary design by Bob Azmon



Issue on FEE development

- Common mode noise issue (ALICE found)



- Common Mode removal is what the on-board DSP for the SAMPA chip is designed to do.
  - But, this is within a chip, i.e. 32 ch
- The technique:
  - Find a large number of “empty channels”.
  - See if they all dip below zero together.
  - Correct everyone up by the amount of the dip.
- ALICE ended up with 5MHZ sampling instead of 10MHz in order to fit the bandwidth of GBTx
  - SAMPA itself can drain all the data

Data rate (two cases)

- Data Rate with zero-suppression
  - 1.42Gbps/board for 30<r<40cm
  - 1.45Gbps/board for 40<r<60cm
  - 0.77Gbps/board for 60<r<80cm
  - → 28Gbps/(1/12 full azimuth)

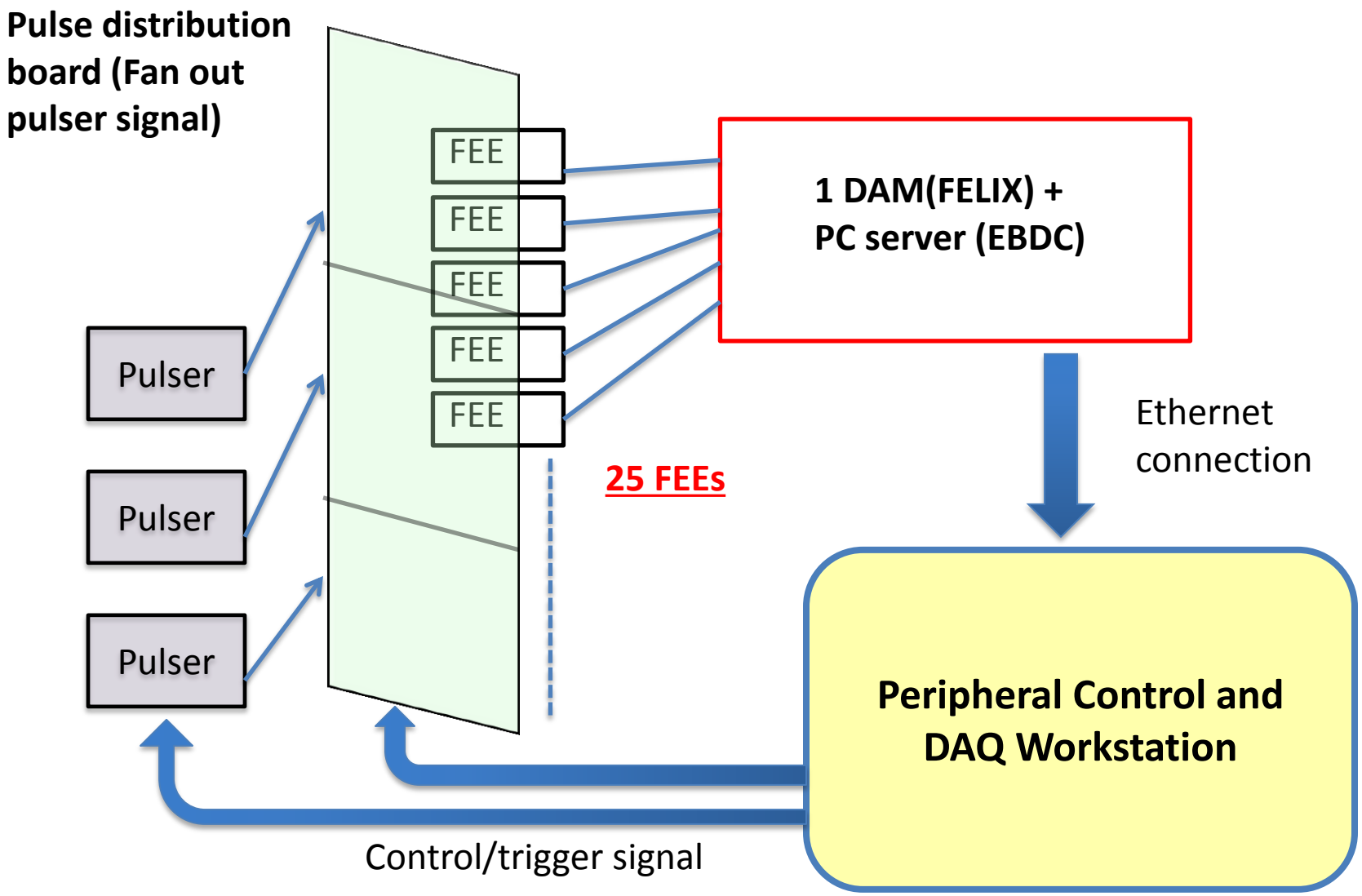
- With no zero-suppression in SAMPA (common-mode noise case)
  - 26Gbps/board (fixed)
    - No way to send this amount of data through one optical link?
  - FPGA on FEE has to do job
    - Need to take care of 11*8 e-links from 8 SAMPAs
    - Average out the charges in pads that have negative values (> 50 pads?)
    - Shift other channels by that amount

- No header is included in the estimate above
  - 40% increase (max) of the data volume for zero-suppression mode
  - Less than 1% increase for non zero-suppression mode

Test stand development

- By the end of June (July?), we should have a set of prototype cards
  - 25 prototype v1 FEEs, 1 FELIX board (already here), 1 EBDC
- We need a test stand to do several testing including chain test
- Additional peripheral for test stand
  - Three pulsers and pulse distribution boards
  - Corresponding to three radial sectors in addition to above
- We have to test 750 FEE cards and 30 DAM boards in the end
  - We have to do this test in 40-60 days (3-4 months). I assume working efficiency is ~50%.
  - Assuming 25 FEEs are tested at one test cycle, we need 30 test cycles
- I propose to make two sets of the board testing setup just in case

Test stand scheme



Costs review for FEE (prototype)

- Total: $60K for v1, and $30K for pre-production

1.2.6.1	TPC FEE Prototype v1						$57,330
1.2.6.1.3	Procure TPC FEE prototype v1 components					$16,500	
		SAMPA chip	CERN	$9,000	200 chips (~$45/chip from Tonko's info) for 25		
		FPGA (Artix-7)	Xilinx	$2,500	Joe's experience (25 boards)		
		Optical transmitter/receiver	Avago	$1,250	Joe's experience (25 boards)		
		Resistor/capacitor/regulator	Digikey	$2,500	Joe's experience (25 boards)		
		Card Connectors	Samtec	$1,250	Joe's experience (25 boards)		
1.2.6.1.4	Fabricate TPC FEE prototype v1 boards					$7,500	
		Initial fee		$5,000	Joe's experience		
		Board fabrication		$2,500	Joe's experience (25 boards)		
1.2.6.1.5	Procure TPC FEE prototype v1 LV power supplies					$5,100	
		MegaPac Chassis (5V)	Vicor West Coast	$5,100	Steve's Quote (Jan, 2016), 1 module		
1.2.6.1.6	Develop TPC FEE Test Stand					$26,980	
		Chain test board fabrication	BNL	$2,000			
		Resistor/capacitor/regulator	Digikey	$100			
		Optical transmitter/receiver	Avago	$50			
		SAMPA chip	CERN	$180	Two chips (with spare of 2)		
		FPGA (Artix-7)	Xilinx	$100	Manufacturer Quote		
		Card Connectors	Samtec	$50			
		Pulser distributor board initial fee	BNL	$2,000			
		Pulser distributor	BNL	$7,500	guess (25 input selectors)		

Costs review for FEE (mass prod.)

- Total: $800K (with power supply and cable), including 25% spare

1.2.6.3	TPC FEE Production						$782,600
1.2.6.3.1	Procure TPC FEE components					$603,000	
		SAMPA chip	CERN	$378,000	4800 + 3600 chips (~$45/chip)		
		FPGA (Artix-7)	Xilinx	$75,000	100 * 600 + 25% spare		
		Optical transmitter/receiver	Avago	$37,500	50 * 600 + 25% spare		
		Resistor/capacitor/regulator	Digikey	$75,000	100 * 600 + 25% spare		
		Card Connectors	Samtec	$37,500	50 * 600 + 25% spare		
1.2.6.3.2	Procure TPC FEE LV power supplies					$62,100	
		10AWG 6T00UP Cable	Belden	$6,000	$1.5/ft, 4000ft.		
		MegaPac chassis (5V)	Vicor West Coast	$56,100	5100 * 10 + 1 spare		
1.2.6.3.3	Fabricate and assemble all TPC Fee boards					$117,500	
		Initial fee		$5,000			
		Board fabrication		$75,000	100 * 600 + 25% spare		
		Parts mounting		$37,500	50 * 600 + 25% spare		

Rough cost estimate (for production)

- Direct M&S cost for 154K channels is 1.3M FY17$
- Development cost is not included. Spare (20-25%) is included
  - Was 1.1M for 100K channel without spare included

Item	# of items	$ per item	$ all
SAMPA Chips	8400	$45	$380K
FEE cards	750	$450	$340K
DAM	30	$8000	$240K
Cables/fibers			$100K
Power Supply	11	$5100	$60K
EBDC	30	$6000	$180K
Total			**$1.3M**

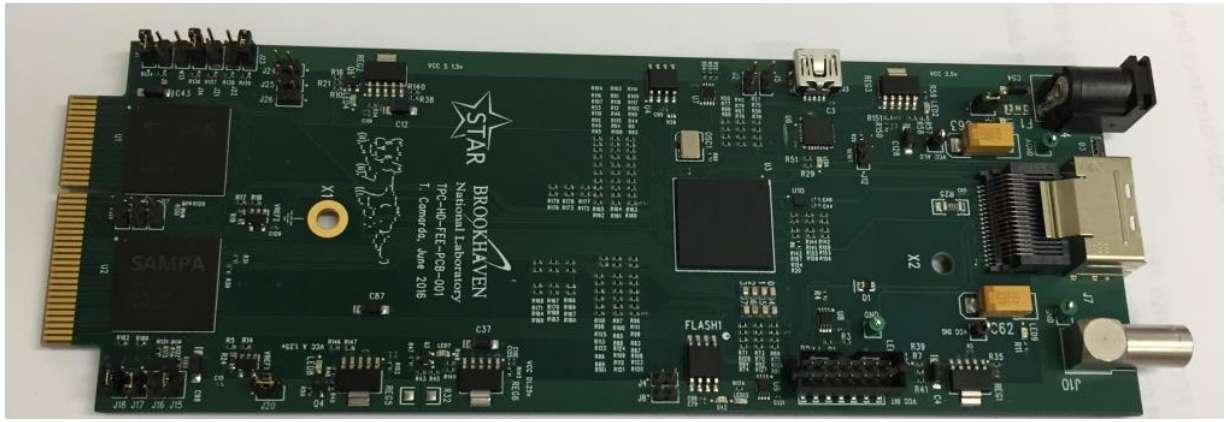
c.f. STAR iFEE is $150/card (64 ch., copper cable readout)

STAR iFEE board

- We have one 64-channel board in hand
  - Data is readable through a USB connector.
  - TS is going to test it next two weeks.

- One more board can be obtained from Tonko

- These boards can be used for magnet testing in June



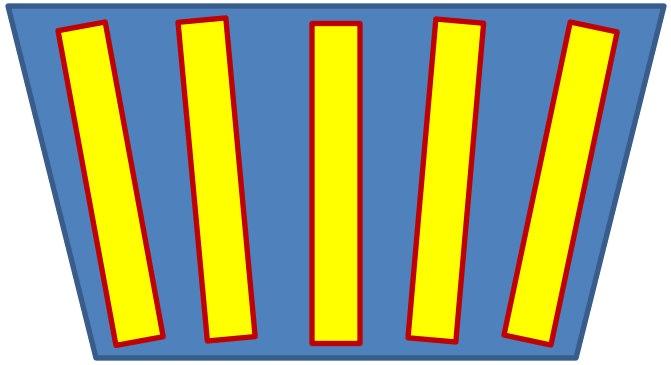
End

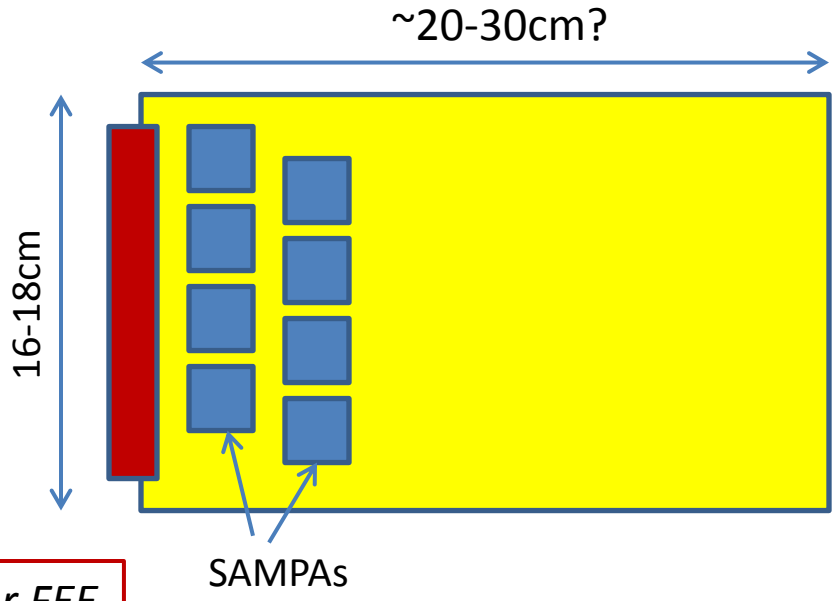
- We are making good progress

Backup

FEE side update

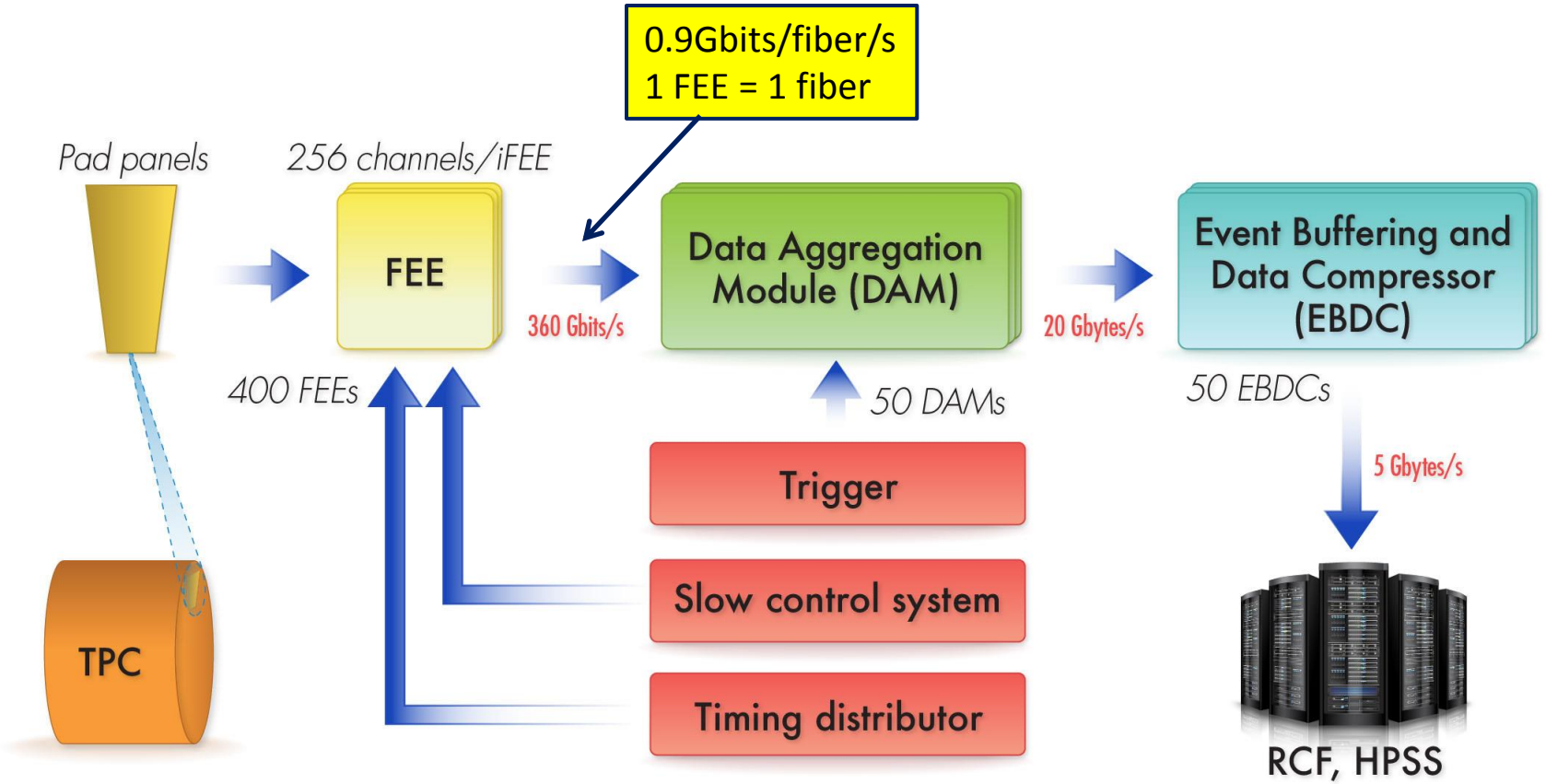
- 256 channels per card (eight SAMPAs) is the fixed number
- From the previous pad layout, the minimum spacing of the FEE cards will be ~2cm (at r=20cm)
  - This is acceptable from the point of view of engineering
- Width of FEE card will be ~16-18cm
  - The most outer radial segment will be 60-78cm
  - Cable from pad to SAMPA should be less than 5 inches (STAR's experience)
- GBT or other protocol?
  - If we put FPGA on the FEE, the optical doesn't need to be GBT
  - FPGA would have SEU. STAR's experience tells one serious SEU event happens every 10 minutes.





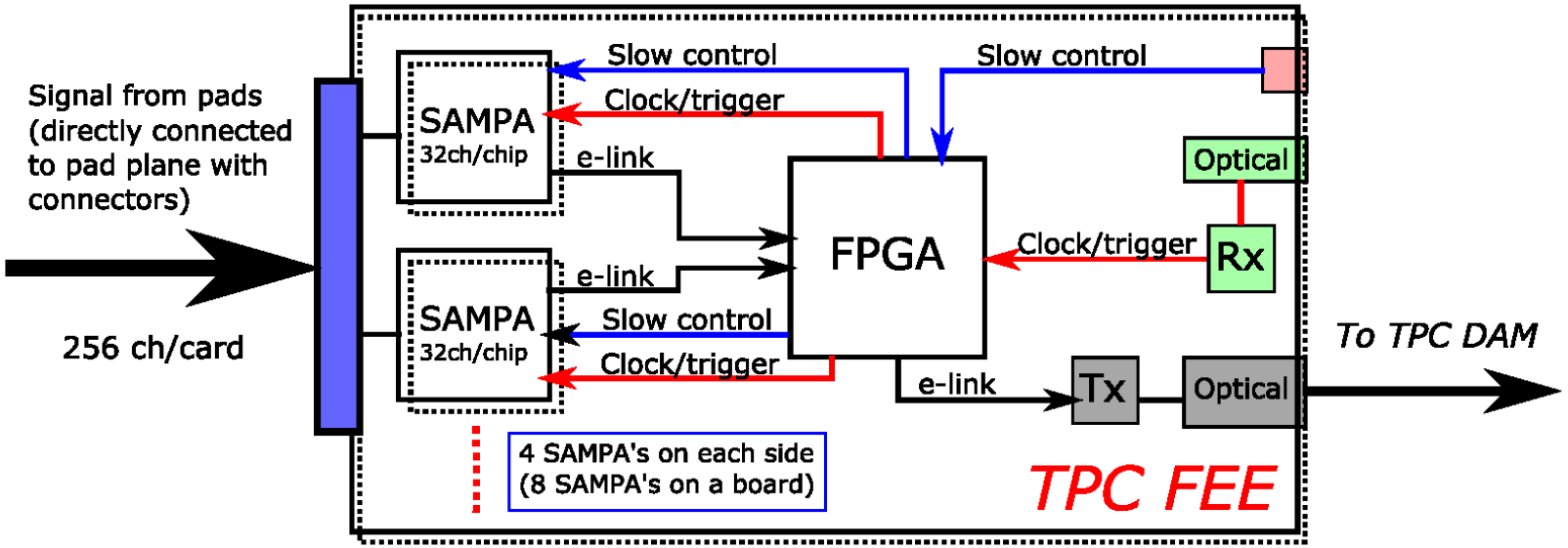
We should start engineering for FEE

Overview of readout chain



FEE (Frontend)

- Each FEE takes care of 256 inputs. 100K ch = 400 FEEs
  - Use of SAMPA chips (SAMPA is “shaper + ADC + DSP”)
  - SAMPA accepts 32 inputs → 8 SAMPAs on a board (4 SAMPAs on each side)
- FPGA receives and distributes slow control and timing/clock signal
- FPGA also collects digitized data from SAMPAs (e-link) and format them for optical transmission



We rely on SAMPA

- SAMPA = CSA + Shaper + ADC + DSP
  - 32 channels input
- Prototype chip became available
  - Final version SAMPA will be available in late 2018

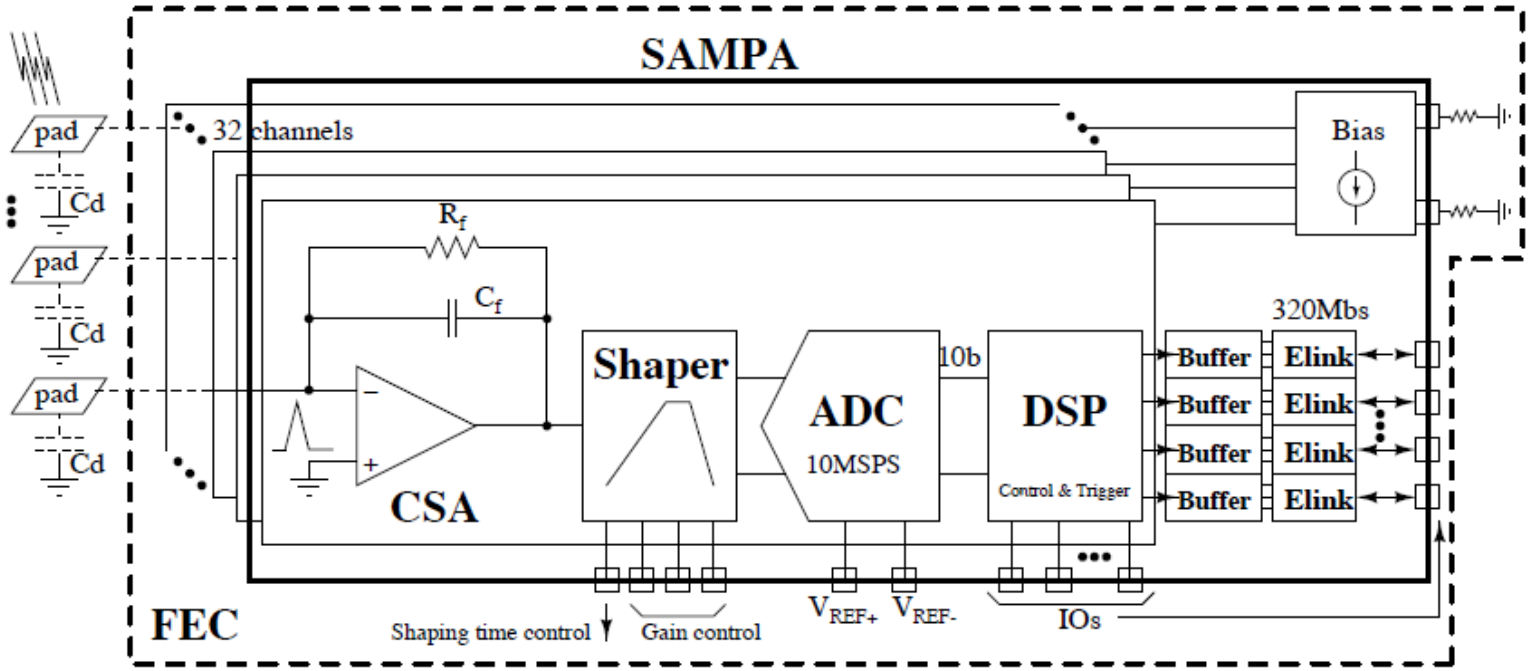
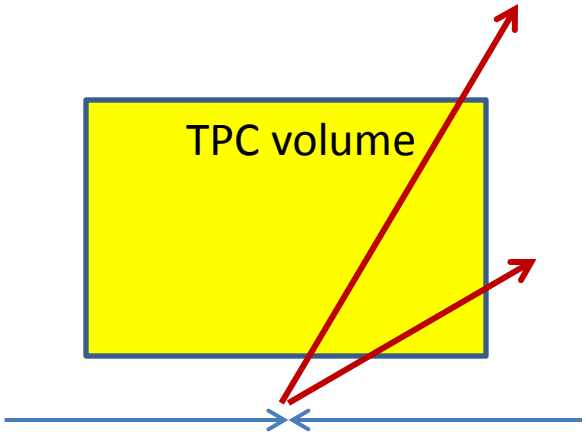


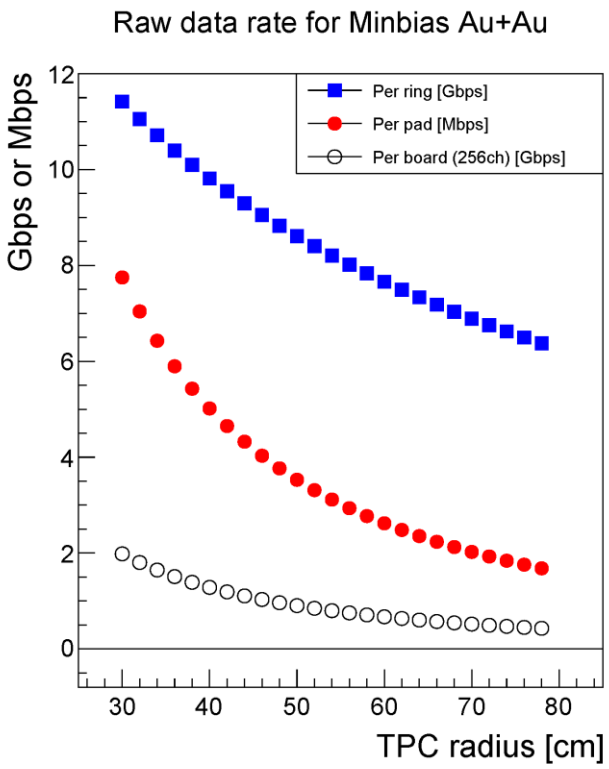
Figure 6.4: Schematic of the SAMPA ASIC for the GEM TPC readout, showing the main building blocks.

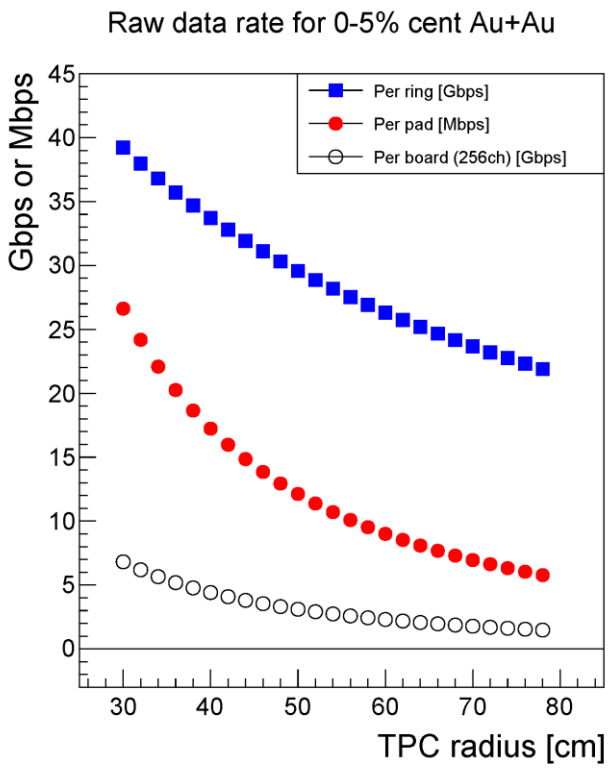
A bit more differential rates

- Radius dependent occupancy and η coverage change are taken into account
- 2 Gbps/board for Minbias, 7 Gbps/board for 0-5% cent Au+Au, @ R= 30cm
  - One board = 256 channels = one optical fiber from FEE to DAM
  - C.f. GBT rate: 4.8 Gbps (line rate), 3.2 Gbps (payload rate)

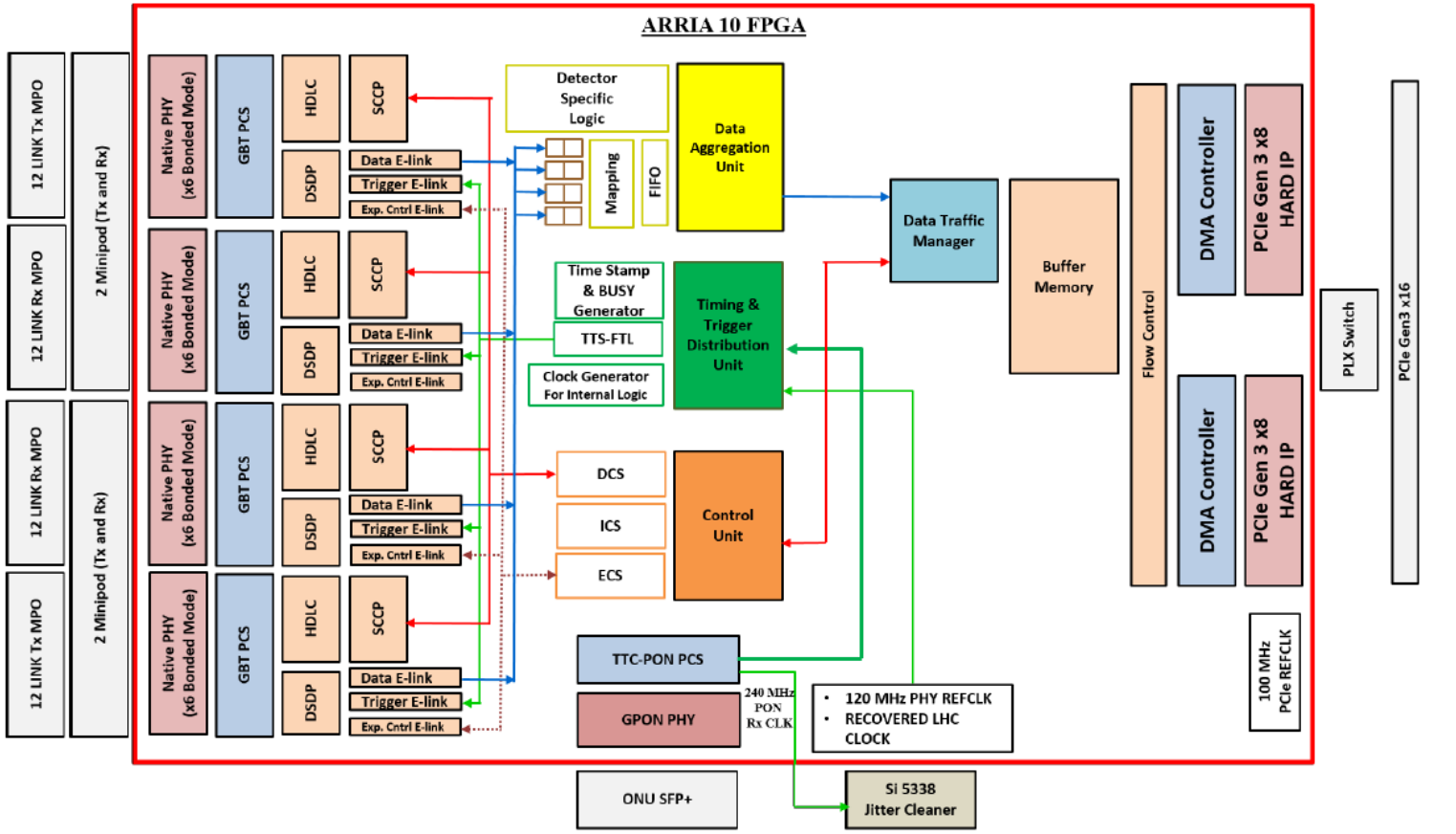
Per ring: Data rate at [r_1, r_1+1cm]







CRU internal logic block connections



JINST 11 (2016) C03021

Cost estimate (for production)

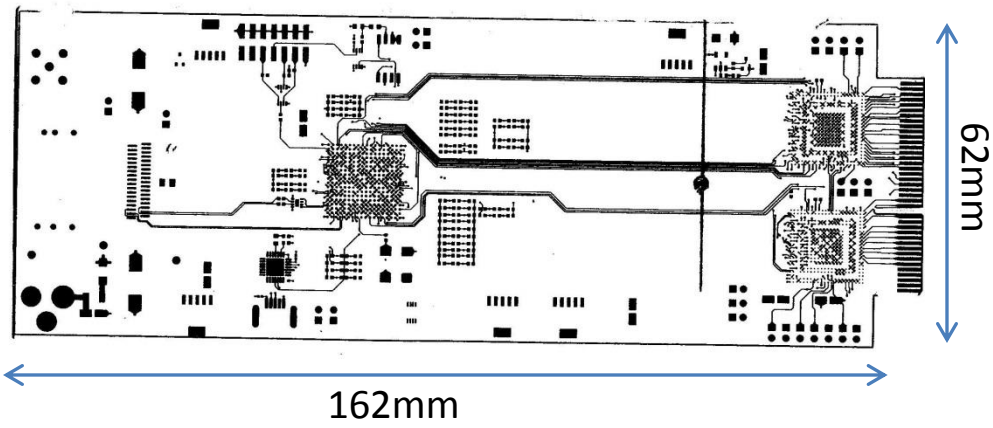
- Direct M&S cost for 100K channels is 1.1M FY16$
- Cost for development is not included.
  - We assumed ~20-30% of this as M&S cost for development

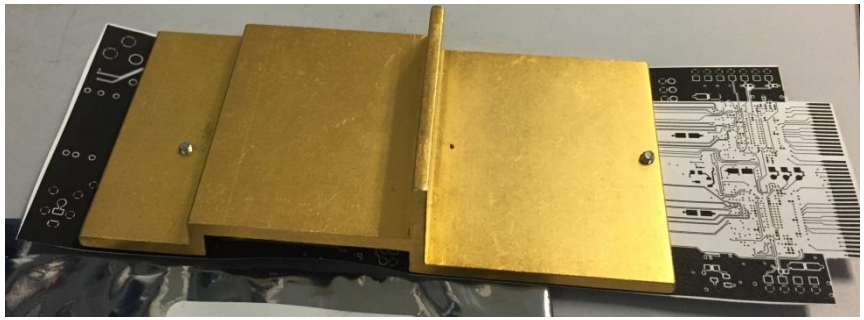
Item	# of items	$ per item	$ all
SAMPA Chips	3200	$44	$140K
FEE cards	400	$700	$280K
DAM	50	$6000	$300K
Cables/fibers			$100K
Power Supply	8	$12000	$100K
EBDC	50	$3000	$150K
Total			**$1.1M**

c.f. STAR iFEE is $150/card (64 ch., copper cable readout)

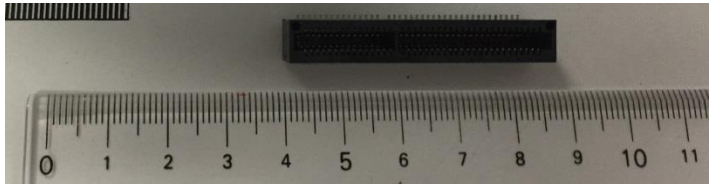
STAR's iFEE

- Good start to think of geometry our front end cards
  - To be attached to pad planes
- Two SAMPA chips on one side of the card
  - Geometry of the card is 62mm*162mm
  - 64 channels/card (32 ch/SAMPA)
  - One SAMPA chip is 15*15mm^2, which is much smaller than I thought
- Input connector is as wide as ~57mm and 10mm in height
  - Takes care of 64 channels. There is one for 160ch also.
- A large heatsink will be attached to the side of the board where no chip is mounted
  - Heatsink is 20mm in height
  - Can be shortened to ~10mm





Input connector (64 channels)



On recording data at 5GB/sec

From Chris Pinkenburg

- 20 week run (12,096,000 sec)
- 5GB/sec → 60.5 PB
- 75% duty factor → 40PB
- 40PB is only a factor of 4 more than STAR took in 2014 using LTO5 tapes/tape drives, should not be a problem in 2022.
- Current LTO7 (released Dec 2015) store 4x data of LTO5 @ 2x write speed

Data rate calculation

- Raw data (100% duty factor is assumed)
  - Sampling rate in z-direction: 10MHz (= 100nsec)
  - Pulse peaking time is 160nsec (fixed from SAMPA's specification), which leads to ~350nsec for whole pulse shape.
    - More than 4 samples in timing (z) direction is necessary. We decided on taking 5 samples including pre-signal
  - One cluster will be spread over 3 pads in r-ϕ plane
    - Coming from the characteristics of the Ne2K (Ne - CF_4 - iC_4H_{10}: 95% - 3% - 2%) gas
  - We measure 30 clusters for one track
  - Each sample is 10 bits: 30 clusters * 15 * 10 bits = 4.5 Kbits/track
  - 800 tracks per event: 4.5Kbits/track * 800 = 3.6 Mbits/event
  - At 100 KHz: 3.6 Mbits/event * 100 KHz = 360 Gbits/s
- Raw → Clustered data: 1 cluster → 8 bytes (following the STAR's case)
  - 15 * 10 bits (raw) → 8 bytes (clustered)
  - 360 Gbits/s (raw) → ~20Gbytes/s (clustered) @ 100KHz